AMENDMENTS TO THE CLAIMS

1 - 23. (Cancelled)

24. (Currently Amended) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a scan in terminal providing an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;

a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern; and

a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to [[~~said~~]]a scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,

whereby said resetting is always performed at said transition time.

25. (Previously Presented) The semiconductor integrated circuit according to Claim 24, further comprising output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode.

26. (Previously Presented) The semiconductor integrated circuit according to Claim 25, further comprising:

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode responsive to said mode signal.

27. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 24, wherein said plurality of flip-flops are serially arranged so as to perform scan testing for said internal logical circuitry.

28. (Previously Presented) The semiconductor integrated circuit according to Claim 24, further comprising transition detection means for detecting the transition time of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition time detection means detects said transition time.

29. (Previously Presented) The semiconductor integrated circuit according to Claim 27, further comprising transition detection means for detecting the transition time of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition time detection means detects said transition time.

30. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 24, wherein said reset control means obtains an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal .

31. (Canceled)

32. (Previously Presented) A method of testing a semiconductor integrated circuit as defined in claim 24, wherein

said plurality of flip-flops are reset at said transition time, between said test mode and said normal mode.

33. (Previously Presented) A method of testing a semiconductor integrated circuit as defined in claim 28, wherein

said plurality of flip-flops are reset at said transition time, between said test mode and said normal mode,.

34. (Canceled)

35. (Previously Presented) The semiconductor integrated circuit as set forth in claim 24 further including a dummy flip-flop in said scan chain that is responsive to a rising and falling of the scan mode signal for resetting said plurality of flip-flops.

36. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

an inputted scan pattern to a scan chain between said scan in terminal and a scan out terminal;

a plurality of flip-flops arranged in said scan chain so as to perform scan testing for said internal logical circuitry responsive to said scan pattern;

a scan mode input providing a scan mode signal for switching said internal logic circuitry between said normal operation state and a scan operation state including said test mode; and

a reset means for resetting said plurality of flip-flops at a transition time, between said test mode and said normal mode, responsive to said scan mode signal for selectively specifying one of said normal operation mode and said test mode by the logical level of said mode signal,

wherein said reset means is responsive to a reset signal inputted from a reset input terminal and resets said plurality of flip-flops at said transition time, between said test mode and said normal mode, in accordance with said mode signal, and further comprising

output control means that is connected serially to said plurality of flip-flops, and which outputs data that is supplied during said test mode while prohibiting the outputting of data that is supplied during said normal operation mode, and

memory means connected to said plurality of flip-flops; and

access control means for prohibiting access to said memory means during said test mode responsive to said mode signal,

whereby said resetting is always performed at said transition time.

37. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 36, wherein said plurality of flip-flops are arranged so as to perform scan testing for said internal logical circuitry.

38. (Previously Presented) The semiconductor integrated circuit according to Claim 36, further comprising transition detection means for detecting the transition time of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition time detection means detects said transition time.

39. (Previously Presented) The semiconductor integrated circuit according to Claim 37, further comprising transition detection means for detecting the transition time of said logical level of said mode signal, wherein said reset means resets said plurality of flip-flops when said transition time detection means detects said transition time.

40. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry as set forth in claim 36, wherein said reset control means obtains an edge detection signal corresponding with the rising edge and the falling edge of the scan mode signal.

41. (Previously Presented) A semiconductor integrated circuit having a normal operation mode and a test mode for scan testing internal logical circuitry, comprising:

a scan path between a scan in source receiving a scan pattern and a scan output with a scan chain including a plurality of scan flip-flops formed between said scan in source and the scan output, said scan flip-flops configured to make scan testing possible according to said scan pattern;

a scan mode signal provided for switching said internal logic circuitry between said normal operation mode and said test mode responsive to said scan mode signal;

a reset input signal for controlling reset of said flip-flops by a reset control block provided to detect a transition time of a logical level of the scan mode signal by an edge detection signal having a pulse length that is at least equal to or greater than one clock period of a system clock, wherein

scan operations are inhibited without resetting at the time of initiating scan operations or normal operations without being reset upon termination of scan operations,

whereby said resetting is always performed at said transition time.

42. (Previously Presented) The semiconductor circuit as set forth in claim 41, further including a dummy flip-flop in said scan path.

43. (Previously Presented) The semiconductor circuit as set forth in claim 41, wherein, during scan testing, said scan pattern is inputted to the scan flip-flops so that by a shift out of said scan chain, data that is to be checked for scan testing are shifted out from the scan output.

44. (Previously Presented) The semiconductor circuit as set forth in claim 41, wherein said reset control block includes a pair of flip-flops and logical output circuits arranged to detect the transition time of a logical level of the scan mode signal.